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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,740	06/20/2003	Umesh Nair	P8987	7379

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,740	NAIR, UMESH	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-12,15-20,23 and 24* is/are rejected.

7)☒ Claim(s) *5,6,13,14,21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

The following claims are objected to because:

(Claim 23) Claim 23 should depend on claim 17.

(Claims 3, 11, and 19) "orphan" in "orphan timing violation" is not clear and not defined in these claims.

(Claims 5, 13, 21) It is not clear how "nominal number of fixes" is obtained and what "nominal number of fixes" represents and it is not clear what to be fixed.

(Claims 5-6, 13-14, 21-22) These claims should clearly define what to be selected in the approach.

(Claims 8, 16, 24) "the buffer" on line 4 lacks antecedent basis.

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 7-12, 15-20, and 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Alpert et al. (US Pub. No. 2004/0123261) who discloses a method/apparatus/system comprising:

(Claim 1 and similarly recited claims 9, 17)

identifying paths and nodes (fig 4A-B, 5A-C, 6A-C, 7-9) within an IC design;

determining node overlap (paragraphs [0012], [0015]-[0017] within the IC design;

calculating possible solutions (fig 7-9) for addressing timing violations within the IC design;

choosing a solution (paragraph [0037], also see "obtain a good solution" in paragraph [0006], "a candidate solution" in paragraph [0032], "obtain a merged solution" in paragraph [0035], "obtain a solution" in paragraph [0048], and "obtain a new solution" in paragraph [0057]-[0058]) for addressing timing violations;

inserting buffers at particular nodes (fig 1A-F, 4A-B, 5A-C, 6A-C) of the IC design; and,

repeating the calculating possible solutions, the choosing a solution and the inserting buffers at particular nodes (paragraphs [0060], [0061], [0063], [0064]) to address timing violations within the IC design.

(Claims 2, 10, 18) wherein the repeating continues until a previous maximum number of violations (i.e., timing constraints, timing slacks, blockage constraints, buffer blockage, arrival time, etc., in paragraph [0006], [0029], [0030], [0037], [0041], [0042]) have been addressed (paragraphs [0060]-[0061], [0063], [0064], also fig 7-9).

(Claims 3, 11, 19) Wherein after the repeating, there are orphan timing violations remaining to be addressed (orphan timing violations are additional timing constraints/problems/over limit at child/children/leaf nodes (i.e., paragraphs [0031], [0032], [0035], [0057], [0058], [0070], [0071], fig 7, 9) that need to be addressed in addition to the violations mentioned in the preceding claims 2, 10, and 18; insofar the limitation is understood.); and, further comprising

inserting buffers at particular locations (fig 1A-F, 4A-B, 5A-C, 6A-C, fig 8-9) to address the orphan timing violations.

(Claims 4, 12, 20) wherein the choosing a solution is based upon fixing a plurality of timing violations based upon various input criteria (various input criteria are, i.e., a number of solutions (paragraph [0012], the number of buffer insertion points and buffer insertion algorithm (paragraph [0038], algorithm strategy (paragraph [0039], search range (paragraph [0048], a number of capacitance/required arrival time pairs (paragraph [0055]), a number of candidate solutions (paragraph [0063]), etc.)

(Claims 7, 15, 23) identifying buffers from a list of potential buffers (buffer library in fig 7) available to insert into the IC design; and

choosing a subset of the buffers (paragraph [0038], [0063], claims 5-6, 13-14) from the list of buffers for inserting at the particular nodes of the IC.

(Claims 8, 16, 24) wherein factors used in choosing a subset of the buffers from the list as buffers include a first order delay characteristic (first order delay characteristic inherently from RC delay (paragraph [0005], [0031]) and/or intrinsic delay (paragraph [0034])) of the buffer, a maximum time slack characteristic (maximum time slack in abstract, paragraphs [0006], [0010], [0027]) of the buffer, and a drive strength characteristic (i.e., load capacitance, source/sink, decoupling and driving of long paths, driving of long wires in paragraphs [0030], [0032], [0041], [0042]) of the buffer.

Allowable Subject Matter

Claims 5-6, 13-14 and 21-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten/amended to overcome the above-mention claim objections and rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 5-6, 13-14 and 21-22 would be allowable because the prior art does not teach or suggest:

(Claims 5, 13, 21) "wherein the various input criteria include a median approach, the median approach including calculating a nominal number of fixes from the calculating possible solutions and then selecting an approach which fixes more than the nominal number of fixes.

(Claims 6, 14, 22) wherein the various input criteria include an acquisitive approach, the acquisitive approach including determining which solution from the calculating possible solutions fixes a greatest number of timing violations and then selecting [the] an approach which fixes the greatest number of timing violations.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Patent Examiner

Paul Dinh
11/15/2004